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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,013	08/20/2003	Koji Naganawa	Y0647.0145	4880

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,013	NAGANAWA, KOJI	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ~~8-20-2003~~. 42104
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt is acknowledged of the Pre-Amendment filed 8-20-2003.

Drawings

Figures 11A - 11E should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2 and 6-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Devanney et al. (US PAT No. 6,243,779).

Regarding claim 1, Figs. 1 and 2 of Devanney et al. teaches a data output circuit which outputs data on an internal bus line (134) onto an external bus line (110), comprising: comparison means (210 in Fig. 2) for comparing data on the external bus

line and data to be output on the internal bus line (col. 6, lines 8-17); inversion means (220 in Fig. 2) for outputting a signal obtained by inverted the data on the internal bus line when the number of changed bits exceed half the total number of bits on the basis of an output result from the comparison means (col. 5, lines 53-64); and control means (230 in Fig. 2) for outputting an inversion display signal (INVERT in Fig. 2) representing that the data has been inverted (col. 6, lines 37-40).

Regarding claim 2, Figs. 1 and 2 of Devanney et al. teaches the circuit according to claim 1 where the comparison means, the inversion means, and the control means constitutes an output data control unit (SENDING CIRCUIT 112 in Fig. 1).

Regarding claim 6, Figs. 1 and 2 of Devanney et al. teaches the circuit according to claim 1 where the data on the internal bus line includes data read out from storage means (SOURCE SUBSYSTEM 114 being memories; col. 4, lines 51-55).

Regarding claim 7, Figs. 1 and 2 of Devanney et al. teaches the circuit according to claim 1 where the comparison means and the control means are arranged for each of groups obtained by classifying internal bus lines into a plurality of groups (210 and 230 arranged for buses 216, 224, INVERT, 424-bits from 110).

Regarding claim 8, Figs. 1 and 2 of Devanney et al. teaches a data output method of outputting data on an internal bus line (134) onto an external bus line (110), comprising the steps of comparing data on the external bus line and data to be output on the internal bus line (210); when the number of changed bits exceeds half the total

number of bits on the basis of a comparison result (col. 5, lines 53-64), inverting (220 in Fig. 2) the data on the internal bus line to output onto the external bus line and outputting a data inversion signal (INVERT in Fig. 2) representing that the data has been inverted (col. 6, lines 37-40).

Regarding claim 9, Figs. 1 and 2 of Devanney et al. teaches the method according to claim 8, where the comparison step comprises the step of receiving a clock signal (CLK in Fig. 4; col. 7, lines 10 -48).

Regarding claim 10, Figs. 1 and 2 of Devanney et al. teaches the method according to claim 8, further comprising the step of reading out the data on the internal bus line from storage means (SOURCE SUBSYSTEM 114 being memories inherently requires a step of reading out; col. 4, lines 51-55).

Regarding claim 11, Figs. 1 and 2 of Devanney et al. teaches the method according to claim 8, where the comparison step comprises the step of performing the comparison step for each of groups obtained by classifying internal bus lines into a plurality of groups, the output step comprise the step of performing the output step for each of groups obtained by classifying internal bus lines into the plurality of groups (210 and 230 arranged for buses 216, 224, INVERT, 424-bits from 110),

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devanney et al. as applied to claims 1-2 above, and further in view of Takasugi (US PAT No. 5,287,327).

Regarding claim 3, Figs. 1 and 2 of Devanney et al. teaches the circuit according to claim 2 where the source subsystem 114 is being a memory and the source subsystem 114 and the sending circuit 112 are being incorporable into a single circuit 116 (col. 4, lines 44-65) , and input/output means (feedback bus in Fig. 2 of Devanney et al.) for transmitting an output data bus signal from the output data control unit as output data onto the external data bus, but does not discloses an amplifier which amplifies read data and data latch means for latching data output from the amplifier. However, Fig. 6 of Takasugi teaches a memory cell array (40) being read out over bus 51 and amplified by AMP 60, and latched by DATA LATCH 70 and output by TRI-STATE OUTUT 80 for the purpose of providing the memory data. Therefore, it would have been obvious at the time of invention to a person in the ordinary skilled in the art to combine the sending circuit of Devanney et al. with the memory circuit of Takasugi in place of the source subsystem 114 of Devanney et la. for the purpose of accessing the data of the memory in reduced switching noise.

Regarding claims 4 and 5, Devanney et al. in view of Takasugi teaches the circuit of according to claim 3 where the input/output means feeds back the output data to the comparison means (the feedback bus to 424 from bus 110 to 210 in Fig. 2 of Devanney et al.), and clock signal supply means (CLK in Fig. 4 of Devanney et al. , CLK in Fig. 6 of Takasugi) for supplying a clock signal to the data latch means, the output

data control unit, and the input/output means.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Walker (US PAT No. 6,046,943) discloses a synchronous semiconductor device output circuit with reduced data switching.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

Date: 11-1-2004